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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/077,093

02/19/2002

Subhash Gupta

CS99-063B

2767

28112

7590

10/03/2003

GEORGE O. SAILE & ASSOCIATES

28 DAVIS AVENUE

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EXAMINER

ERDEM, FAZLI

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/077,093

Applicant(s)

GUPTA ET AL.

Examiner

Fazli Erdem

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 17-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 17-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 17-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. (6,235,600) in view of Ding et al. (6,153,472) further in view of Krivokapic (5,559,357) further in view of Lee et al. (6,033,981).

Regarding Claims 17-21, Chiang et al. show a method for improving hot carrier lifetime via a nitrogen implantation procedure preformed before or after a TEOS liner deposition where a process for fabricating input/output, N channel devices, featuring an ion implanted nitrogen region used to reduce hot carrier electron injection is shown. The process features implanting a nitrogen region, at the interface of an overlying silicon dioxide layer, and an underlying lightly doped region. The implantation procedure can either be performed prior to or after the deposition of a silicon oxide liner layer, in both cases resulting in a desire nitrogen pile-up at the oxide-lightly doped interface, as well as resulting in a more graded lightly doped source/drain profile. Furthermore, Figs. 1-7 show insulator, polysilicon layer, oxide liner, L-Shaped nitride spacer in a required manner. Chiang et al. fail to disclose the oxide, liner/sidewall, and polysilicon traces in the required manner. However, Ding et al. disclose a method for fabricating a flash memory where the oxide structure is disclosed in the required manner. Furthermore, Krivokapic discloses a poly LD self-aligned channel transistors where the required liner/sidewall

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structure in the required manner is shown. Lee et al. disclose a keyhole-free process for high aspect ratio gap filing where the required polysilicon trace structure is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the oxide, liner/sidewall, and polysilicon traces in the required manner in Chiang et al. as taught by Ding et al., Krivokapic, and Lee et al. respectively in order to have a semiconductor device with better performance.

2. Claims 22-25 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. (6,235,600) in view of Ding et al. (6,153,472) further in view of Chen et al. (6,323,105) further in view of Krivokapic (5,559,357) further in view of Thomas (6,590,265).

Regarding Claims 22-25, Chiang et al. and Ding et al. fail to disclose the polysilicon structure, line/sidewall, and polysilicon trace structure in the required manner. However, Chen et al. disclose a method for fabricating an isolation structure including a shallow trench isolation structure and a local-oxidation isolation structure where the required polysilicon structure is disclosed. Furthermore, Krivokapic discloses a poly LD self-aligned channel transistors where the required liner/sidewall structure in the required manner is shown. Thomas discloses semiconductor device with sidewall spacers having minimized area contacts where the required polysilicon trace structure is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the polysilicon structure, liner/sidewall, and polysilicon/trace structure in required manner in Chiang et al. and Ding et al. combination as taught by Chen et al., Krivokapic, and Thomas respectively in order to have a semiconductor device with better performance.

3. Claims 26-28 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. (6,235,600) in view of Ding et al. (6,153,472) further in view of Tsai (6,251,748) further in view of Krivokapic (5,559,357) further in view of Thomas (6,590,265).

Regarding Claims 26-28, Chiang et al. and Ding et al. fail to disclose the polysilicon structure in the required manner, liner/sidewall structure in the required manner and the polysilicon trace structure in the required manner. However, Tsai discloses a method of manufacturing shallow trench isolation structure where the required polysilicon structure is disclosed. Furthermore, Krivokapic discloses a poly LD self-aligned channel transistors where the required liner/sidewall structure in the required manner is shown. Thomas discloses semiconductor device with sidewall spacers having minimized area contacts where the required polysilicon trace structure is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the polysilicon structure, liner/sidewall, and polysilicon/trace structure in required manner in Chiang et al. and Ding et al. combination as taught by Tsai, Krivokapic, and Thomas respectively in order to have a semiconductor device with better performance.

Conclusion

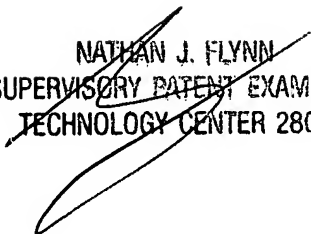
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (703) 305-3868. The examiner can normally be reached on M - F 8:00 - 5:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

FE


NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800